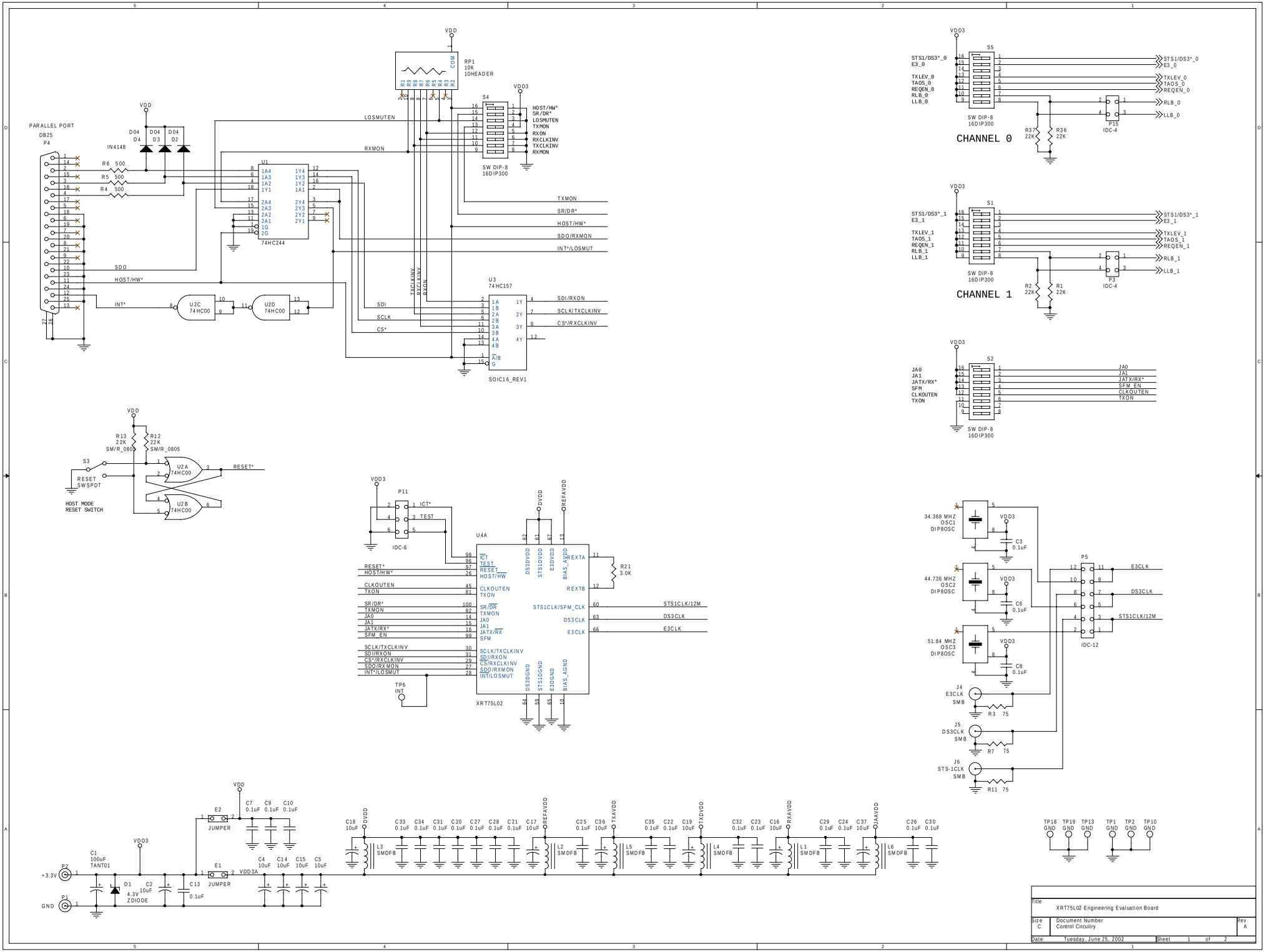
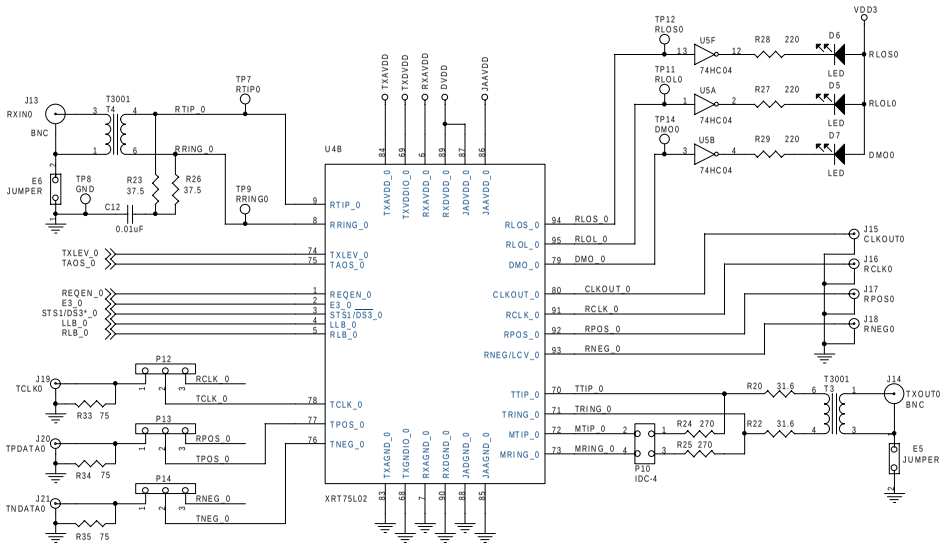
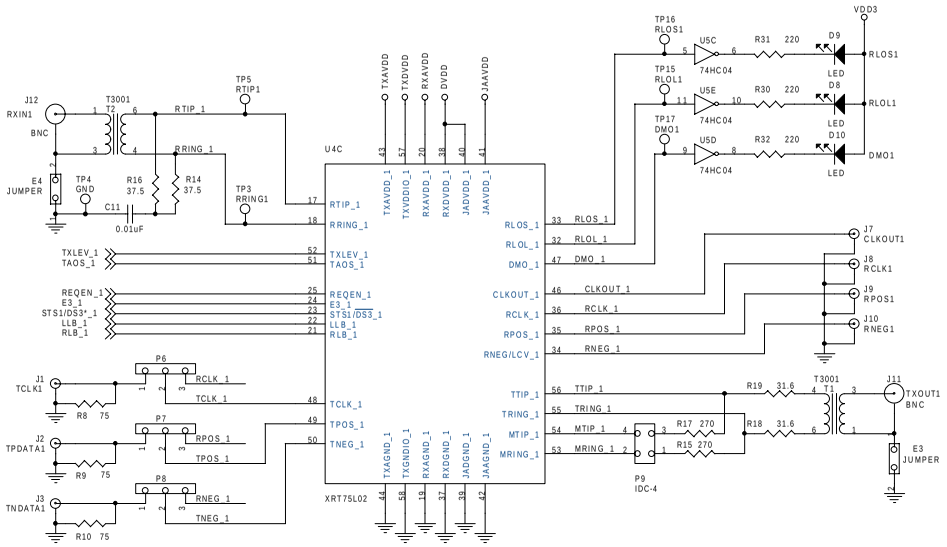

PARALLEL PORT
DB25
P4
VDD
D04
D4
D3
D2
IN4148
R6 500
R5 500
R4 500
U1
74HC244
LOSMUTEN
RXMON
RP1
10K
10HEADER
S4
SW DIP-8
16DIP300
HOST/HW*
SR/DR*
LOSMUTEN
TXMON
RXON
RXCLKINV
TXCLKINV
RXMON
TXMON
SR/DR*
HOST/HW*
SDO/RXMON
INT*/LOSMUT
SDO
HOST/HW*
INT*
U2C
74HC00
U2D
74HC00
U3
74HC157
SDI
SCLK
CS*
SDI/RXON
SCLK/TXCLKINV
CS*/RXCLKINV
SOIC16_REV1
S5
VDD3
STS1/DS3*_0
E3_0
TXLEV_0
TAOS_0
REQEN_0
RLB_0
LLB_0
SW DIP-8
16DIP300
R37
22K
R36
22K
P15
IDC-4
CHANNEL 0
S1
STS1/DS3*_1
E3_1
TXLEV_1
TAOS_1
REQEN_1
RLB_1
LLB_1
R2
22K
R1
22K
P3
IDC-4
CHANNEL 1
S2
JA0
JA1
JATX/RX*
SFM
CLKOUTEN
TXON
JATX/RX*
SFM_EN
R13
22K
SM/R_080
R12
22K
SM/R_0805
S3
RESET
SWSPDT
HOST MODE
RESET SWITCH
U2A
74HC00
U2B
74HC00
RESET*
P11
ICT*
TEST
IDC-6
U4A
DVDD
REFAVDD
RESET*
HOST/HW*
CLKOUTEN
TXON
SR/DR*
TXMON
JA0
JA1
JATX/RX*
SFM_EN
SCLK/TXCLKINV
SDI/RXON
CS*/RXCLKINV
SDO/RXMON
INT*/LOSMUT
REXTA
REXTB
R21
3.0K
STS1CLK/SFM_CLK
DS3CLK
E3CLK
STS1CLK/12M
TP6
INT
XRT75L02
34.368 MHZ
OSC1
DIP8OSC
C3
0.1uF
44.736 MHZ
OSC2
DIP8OSC
C6
0.1uF
51.84 MHZ
OSC3
DIP8OSC
C8
0.1uF
P5
IDC-12
J4
E3CLK
SMB
R3 75
J5
DS3CLK
SMB
R7 75
J6
STS-1CLK
SMB
R11 75
P2
+3.3V
P1
GND
C1
100uF
TANT01
D1
4.3V
ZDIODE
C2
10uF
C13
0.1uF
E2
JUMPER
E1
JUMPER
VDD3A
C7
0.1uF
C9
0.1uF
C10
0.1uF
C4
10uF
C14
10uF
C15
10uF
C5
10uF
C18
10uF
L3
SMDFB
C33
0.1uF
C34
0.1uF
C31
0.1uF
C20
0.1uF
C27
0.1uF
C28
0.1uF
C21
0.1uF
C17
10uF
L2
SMDFB
C25
0.1uF
C36
10uF
L5
SMDFB
C35
0.1uF
C22
0.1uF
C19
10uF
L4
SMDFB
C32
0.1uF
C23
0.1uF
C16
10uF
L1
SMDFB
C29
0.1uF
C24
0.1uF
C37
10uF
L6
SMDFB
C26
0.1uF
C30
0.1uF
TP18
GND
TP19
GND
TP13
GND
TP1
GND
TP2
GND
TP10
GND
Title
XRT75L02 Engineering Evaluation Board
Size
C
Document Number
Control Circuitry
Rev
A
Date:
Tuesday, June 25, 2002
Sheet
1
of
2





Title	XRT75L02 Engineering Evaluation Board	
Size C	Document Number Channels 0 and 1	Rev A
Date: Tuesday, June 25, 2002	Sheet 2 of 2	